REMARKS

Claims 1-15 are presently pending and stand rejected. Claims 16-18 are cancelled without prejudice.

Claims 1-13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Malladi in view of Sugiyama.

Claims 14 and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Malladi in view of Sugiyama and Son.

Claim 14, 16, and 18 were "rejected under 35 U.S.C. § 112, ¶2, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention." Office Action, at 2.

Claims 1 and 7 were rejected under 35 U.S.C. § 103(a) as being obvious from Malladi in view of Sugiyama. Examiner has indicated that "Malladi is silent in regards to writing a start code starting at a byte in a middle portion of a data word in a memory. However, Sugiyama teaches writing a start code starting at a byte in a middle portion of a data word in a memory. However, Sugiyama teaches writing a start code starting at a byte in a middle portion of a data word in a memory ([0123] and fig. 13A and 14).".

Assignee respectfully traverse the rejection. Although in Figure 13A, "each code boundary is byte assigned", Paragraph 0119, there is no teaching that the byte is "in a middle portion of a data word". Moreover, 0123 teaches that "Fig 14 shows a real example of a header of an MPEG stream". Note that since Figure 14 merely describes the stream, without any reference to how the stream is stored in memory, the foregoing does not teach "a start code starting at a byte in a middle portion of a data word in a memory".

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Accordingly, for at least the foregoing reason, Assignee respectfully traverses the rejection to claims 1 and 7 and request that Examiner withdraw them, as well as the rejection to claims 2-6 and 8-15.

Additionally, claims 1 and 7 are now amended to recite, among other limitations, "fetching data from the memory starting from the byte in the middle portion of the data word". Although Examiner has indicated that Malladi teaches "fetching data from the memory starting from the byte (column 15, line 39-41 and fig. 4)" there is no teaching of "fetching data from the memory starting from the byte in the middle portion of the data word".

Accordingly, for at least the foregoing reason, Assignee respectfully traverses the rejection to claims 1 and 7 and request that Examiner withdraw them, as well as the rejection to claims 2-6 and 8-15.

Additionally, claim 14 was under 35 U.S.C. § 112. Assignee respectfully traverses the rejection because Assignee is not required to limit the claim to either of "the address is loaded into a register based from the least significant bit" or not, and respectfully submits that the claim language speaks for itself.

CONCLUSION

For at least the foregoing reasons, Assignee submits that each of the pending claims are now in a condition for allowance. Accordingly, Examiner is requested to pass this case to issuance.

It is believed that all monies for the actions described herein are provided with this correspondence. To the extent

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Deleted: .Accordingly, Assignee respectfully traverse the rejection to claim 1, as well as to dependent claims 2-6.¶ .Claim 7 was rejected under 35 U.S.C. § 103(a) as being obvious from the combination of Malladi in view of Sugiyama. Claim 7 recites, among other limitations, "storing a start code at a byte in a middle portion of a particular one of the data words" and "providing data from the memory starting from the starting address". For at least the reasons indicated in claim 1, Assignee respectfully traverses the rejection to claim 7.¶ .Additionally, claim 7 recites, among other limitations, "a direct memory access module". Examiner has indicated that Malladi teaches "a direct memory access module for providing data from the memory starting from the starting address (Malladi, column 21-24)". Assigne ... [2]

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that additional monies are required for any of the actions requested in the correspondence, Commissioner is authorized to charge such fees and credit any overpayments to deposit account 13-0017.

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Respectfully Submitted

September 2, 2008

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16. (Currently Amended) A direct memory access module for providing video data from a starting address to an ending address, said direct memory access module comprising:

a buffer comprising a plurality of data words for storing the video data from the starting address and the ending address;

a first masking register for discarding a portion of a first data structure that precedes the starting address, the first masking register comprises a plurality of bytes corresponding to byte positions of the data words; and

a state machine for loading the first masking register with a pattern wherein each byte of the plurality of bytes in the first mask register that corresponds to a byte position that is less than the four least significant bits of the starting address are loaded with a first value, and wherein each byte of the plurality of bytes in the first mask register that corresponding corresponds to a byte position that is equal or greater than the four least significant bits of the starting address are loaded with a second value.

17. (Original) The direct memory access module of claim 14, wherein the first value is a hexadecimal 0 and wherein the second value is a hexadecimal F, and further comprising:

an arithmetic logic unit for performing a logical AND operation between a first one of the plurality of data words in the buffer and the first masking register.

18. (Currently Amended) The direct memory access module of claim 14, further comprising:

a second masking register for discarding a portion of a second data structure that follows the ending address, the second masking register comprising a plurality of bytes corresponding to byte positions of the data words; and

a state machine for loading the second masking register with a pattern wherein each byte of the plurality of bytes in the second mask register that corresponds to a byte position that is less than or equal to the four least significant bits of the ending address are loaded with the second value, and wherein each byte of the plurality of bytes in the second mask register that corresponds to a byte position that is greater than the four least significant bits of the ending address are loaded with the first value.

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Accordingly, Assignee respectfully traverse the rejection to claim 1, as well as to dependent claims 2-6.

Claim 7 was rejected under 35 U.S.C. § 103(a) as being obvious from the combination of Malladi in view of Sugiyama. Claim 7 recites, among other limitations, "storing a start code at a byte in a middle portion of a particular one of the data words" and "providing data from the memory starting from the starting address". For at

least the reasons indicated in claim 1, Assignee respectfully traverses the rejection to claim 7.

Additionally, claim 7 recites, among other limitations, "a direct memory access module". Examiner has indicated that Malladi teaches "a direct memory access module for providing data from the memory starting from the starting address (Malladi, column 21-24)". Assignee calls Examiner's attention to the fact that Malladi appears to have only 22 columns. Moreover, there is nothing in columns 21-22 that would suggest a "direct memory access module". Accordingly, Assignee respectfully traverse the rejection to claim 7 for at least this reason as well.

Additionally, claim 14 was rejected under 35 U.S.C. § 103(a) as being obvious from Malladi in view of Sugiyama, in view of Son. Examiner indicated that "wherein the direct memory access module (Malladi, column 21-24) further comprises: a buffer comprising a plurality of data words for storing the video data from the starting address (Malladi, Malladi discloses where the parameters are loaded into a predefine memory location, column 7, line 63 to column 8, line 1-8." Malladi, Col. 8, Lines 3-5 describe "a quantization matrix identified in sequence header 14 is loaded into a predefined memory location on a video core (VCORE).

Assignee respectfully traverses because Malladi does not disclose the VCORE as part of a direct memory access module. Accordingly, Malladi does not teach "the direct memory access module further comprises: a buffer".

Examiner is respectfully requested to withdraw the rejection to claim 14 as well as to dependent claim 18.

Assignee traverse the rejection to claim 16 and 17 for at least the same reasons indicated in claim 14.

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Claims 14, 16, and 18 are amended. Assignee will attempt to explain the claims. There is a "masking register … comprises a plurality of bytes corresponding to byte positions of the data words". The state machine loads the "first masking register with a pattern". "[E]ach byte of the plurality of bytes in the first mask register that corresponds to a byte position that is less than the four least significant bits of the starting address are loaded with a first value" and "each byte of the plurality of bytes in the first mask register that corresponds to a byte position that is equal or greater than the four least significant bits of the starting address are loaded with a second value".